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Title of Documents Transmitted: Brief on Appeal

Applicants:	Osborn et al.
Appl. No.:	09/726,831
Filing Date:	11/30/2000
Art Unit:	2676
Atty. Dkt. No.:	035451-0198 (3550.Palm)

By: Chad E. Bement
Name: Chad E. Bement
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Roberta A. Cooper
Roberta A. Cooper

Atty. Dkt. No. 035451-0198 (3550.Palm)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Applicant: Osborn et al.

Title: CONTROL OF COLOR DEPTH IN A COMPUTING DEVICE

Appl. No.: 09/726,831

Filing Date: 11/30/2000

Examiner: Quillen, Allen E.

Art Unit: 2676

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BRIEF ON APPEAL TRANSMITTAL

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Sir:

Transmitted herewith are the following documents for the above-identified application.

[X] Brief On Appeal (22 pages).

[X] Please charge Deposit Account No. 06-1447 in the amount of $500.00. A duplicate copy of this transmittal is enclosed. The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 06-1447. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 06-1447.

Respectfully submitted,

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BRIEF ON APPEAL

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Sir:

Under the provisions of 37 C.F.R. § 41.37, this Appeal Brief is being filed together with a check in the amount of $500.00 covering the 37 C.F.R. 41.20(b)(2) appeal fee. If this fee is deemed to be insufficient, authorization is hereby given to charge any deficiency (or credit any balance) to the undersigned deposit account 06-1447.

This paper is being filed in response to the final Office Action dated July 1, 2005 (finally rejecting claims 1-13 and 15-30). The Notice of Appeal was filed on October 3, 2005. Applicants respectfully request favorable reconsideration of the application.

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1. REAL PARTY IN INTEREST

The real party in interest is the assignee of record, Palm, Inc. (as recorded in the records of the United States Patent and Trademark Office at Reel/Frame 011426/0301 on November 30, 2000).

2. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences that will directly affect, be directly affected by, or have a bearing on the present appeal, that are known to Appellants or Appellants' patent representative.

3. STATUS OF CLAIMS

This is an appeal from the final Office Action dated July 1, 2005, finally rejecting claims 1-13 and 15-30. Claims 1-13 and 15-30 are on appeal.

4. STATUS OF AMENDMENTS

Claims 1-13 and 15-30 were pending in the application when a final Office Action dated July 1, 2005 was issued. No claims have been amended in the present application subsequent to the receipt of the final Office Action dated July 1, 2005.

5. SUMMARY OF CLAIMED SUBJECT MATTER

The present application relates generally to memory architecture for computing devices including display logic that is configured to manage the memory and allocate the memory according to a display mode. See Specification, page 2, lines 10-12.

Independent claim 1 is directed to a computing device (100). See Specification, page 4, lines 12-22 and Fig. 1. The computing device (100) includes a communications bus (210), and a display (209) configured to display in more than one display mode (See Specification, page 7, lines 1-17) and coupled to the communications bus (210) (See Fig. 2). The computing device

(100) also includes a processor (201), coupled to the display (209) and to the communications bus (210) (See Fig. 2), and a display controller (205) coupled to the communications bus (210) (See Specification, page 6, lines 1-2 and Fig. 2) and having dedicated internal display random access memory (212) (See Specification, page 6, lines 8-9). The internal display random access memory (212) is used for storing display information (See Specification, page 6, line 27-page 7, line 1). The internal display random access memory (212) is configured to receive and provide access to display information to be communicated to the display (See Specification, page 6, line 27-page 7, line 17). The internal display random access memory (212) is controlled by display logic (See Specification, page 6, line 27-page 7, line 17). The computing device (100) also includes a dedicated external display random access memory (211) coupled to the display controller (See Specification, page 6, lines 1-9). The display logic is configured to manage the internal (212) and external (211) display random access memory and allocate the internal (212) and external (211) display random access memory across the internal (212) and external (211) display random access memory according to the display mode (See Specification, page 7, lines 1-5). The display logic is configured to change the display mode during operation of an application running on the computing device (100) according to changing graphical needs of the application (See Specification, page 7, lines 5-17). The display modes include at least one of resolution modes and color modes (See Specification, page 7, lines 5-17).

Independent claim 15 is directed to a personal digital assistant (100). See Specification, page 4, lines 12-22 and Fig. 1. The personal digital assistant (100) includes a communication bus (210) and a display (209) configured to display in more than one display mode (See Specification, page 7, lines 1-17) and coupled to the communications bus (210) (See Fig. 2). The personal digital assistant (100) also includes a processor (201), coupled to the display (209) and to the communications bus (210) (See Fig. 2), and a display controller (205) coupled to the communications bus (210) (See Specification, page 6, lines 1-2 and Fig. 2) and having dedicated internal display random access memory (212) (See Specification, page 6, lines 8-9). The internal display random access memory (212) is used for storing display information (See Specification, page 6, line 27-page 7, line 1). The internal display random access memory (212) is configured

to receive and provide access to display information to be communicated to the display (See Specification, page 6, line 27-page 7, line 17). The internal display random access memory (212) is controlled by display logic (See Specification, page 6, line 27-page 7, line 17). The personal digital assistant (100) also includes a dedicated external display random access memory (211) coupled to the display controller (See Specification, page 6, lines 1-9). The display logic is configured to manage the internal (212) and external (211) display random access memory and allocate the internal (212) and external (211) display random access memory across the internal (212) and external (211) display random access memory according to the display mode (See Specification, page 7, lines 1-5). The display logic is configured to change the display mode during operation of an application running on the computing device (100) according to changing graphical needs of the application (See Specification, page 7, lines 5-17). The display modes include at least one of resolution modes and color modes (See Specification, page 7, lines 5-17).

Independent claim 22 is directed to a computing device (100). See Specification, page 4, lines 12-22 and Fig. 1. The computing device (100) includes a communications bus (210) and a display (209) configured to display in more than one display mode (See Specification, page 7, lines 1-17) and coupled to the communications bus (210) (See Fig. 2). The computing device (100) also includes a processor (201), coupled to the display (209) and to the communications bus (210) (See Fig. 2), and a display controller (205) coupled to the communications bus (210) (See Specification, page 6, lines 1-2 and Fig. 2) and having dedicated internal display random access memory (212) (See Specification, page 6, lines 8-9). The internal display random access memory (212) is used for storing display information (See Specification, page 6, line 27-page 7, line 1). The internal display random access memory (212) is configured to receive and provide access to display information to be communicated to the display (See Specification, page 6, line 27-page 7, line 17). The internal display random access memory (212) is controlled by display logic (See Specification, page 6, line 27-page 7, line 17). The computing device (100) also includes a dedicated external display random access memory (211) coupled to the display controller (See Specification, page 6, lines 1-9). The display logic being configured to manage the internal (212) and external (211) display random access memory and allocate the internal

(212) and external (211) display random access memory across the internal (212) and external (211) display random access memory according to the display mode (See Specification, page 7, lines 1-5). The display logic is configured to change the display mode during operation of an application running on the computing device (100) according to changing graphical needs of the application (See Specification, page 7, lines 5-17). The display modes include at least one of resolution modes and color modes (See Specification, page 7, lines 5-17).

6. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The issue on appeal is whether claims 1-13 and 15-30 may properly be rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,915,265 ("Crocker et al.") in view of U.S. Patent No. 5,793,385 ("Nale") and U.S. Patent No. 5,712,664 ("Reddy").

7. ARGUMENT

I. LEGAL STANDARDS

All claim rejections at issue in this appeal are made under 35 U.S.C. § 103(a)[1] The legal standards under 35 U.S.C. § 103(a) are well-settled.

Obviousness under 35 U.S.C. § 103(a) is a legal conclusion involving four factual inquiries:

(1) the scope and content of the prior art;

(2) the differences between the claims and the prior art;

(3) the level of ordinary skill in the pertinent art; and

(4) secondary considerations, if any, of non-obviousness.

[1] "A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made." 35 U.S.C. §103(a).

Litton Systems, Inc. v. Honeywell, Inc., 87 F. 3d 1559, 1567, 39 U.S.P.Q. 2d 1321, 1325 (Fed. Cir. 196). See also Graham v. John Deere Co., 383 U.S. 1, 148 U.S.P.Q. 459 (1966).

In proceedings before the Patent and Trademark Office (PTO), the Examiner bears the burden of establishing a prima facie case of obviousness based upon the prior art. In re Piasecki, 745 F.2d 1468, 1471-72, 223 U.S.P.Q. 785, 787-88 (Fed. Cir. 1984). A prima facie case of obviousness requires that the prior art reference or references teaches or suggests all of the claimed limitations. In re Royka, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974). "The Examiner can satisfy this burden only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references. In re Fritch, 972 F.2d 1260 (Fed. Cir. 1992); In re Fine, 837 F.2d 1071, 1074 (Fed. Cir. 1988); In re Lalu, 747 F.2d 703,705, 223 U.S.P.Q. 1257, 1258 (Fed. Cir. 1984); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 297 n.24, 227 U.S.P.Q. 657, 667 n.24 (Fed. Cir. 1985); ACS Hospital Systems, Inc. v. Montefiore Hospital, 782 F.2d 1572, 1577, 221 U.S.P.Q. 929, 933 (Fed. Cir. 1984). It is improper to combine references where the references teach away from their combination. See In re Grasselli, 713 F.2d 731, 743, 218 U.S.P.Q. 769, 779 (Fed. Cir. 1983). When a reference teaches away from the claimed invention, that teaching is strong evidence of non-obviousness. See U.S. v. Adams, 383 U.S. 39, 148 U.S.P.Q. 79 (1966); In re Royka, 490 F. 2d 981, 180 U.S.P.Q. 580 (CCPA 1974). If the proposed combination of the references would change the principle of operation of the reference being modified, the teachings of the references are not sufficient to render the claims prima facie obvious. See In re Ratti, 270 F.2d 810, 123 U.S.P.Q. 349 (C.C.P.A. 1959).

As noted by the Federal Circuit, the "factual inquiry whether to combine references must be thorough and searching." McGinley v. Franklin Sports, Inc., 262 F.3d 1339, 60 USPQ.2d 1001 (Fed. Cir. 2001). Further, it "must be based on objective evidence of record." In re Lee, 277 F.3d 1338, 61 USPQ.2d 1430 (Fed. Cir. 2002). The teaching or suggestion to make the claimed combination must be found in the prior art, and not in the applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ.2d 1438 (Fed. Cir. 1991). The mere fact that references can be

combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. In re Mills, 916 F.2d 680, 16 USPQ.2d 1430 (Fed. Cir. 1990). "It is improper, in determining whether a person of ordinary skill would have been led to this combination of references, simply to '[use] that which the inventor taught against its teacher.'" Lee (citing W.L. Gore v. Garlock, Inc., 721 F.2d 1540, 1553, 220 USPQ 303, 312-13 (Fed. Cir. 1983)).

II. REJECTION OF CLAIMS 1-13 AND 15-30 UNDER 35 U.S.C. § 103(a) BASED ON CROCKER ET AL. IN VIEW OF NALE AND REDDY

In the final Office Action dated July 1, 2005, the Examiner rejected claims 1-13 and 15-30 under 35 U.S.C. § 103(a) as being unpatentable over Crocker et al. in view of Nale and Reddy.

Claim 1 is in independent form and claims 2-13 depend from claim 1.

Claim 15 is in independent form and claims 16-21 depend from claim 15.

Claim 22 is in independent form and claims 23-30 depend from claim 22.

The Examiner's rejection of claims 1-13 and 15-30 under 35 U.S.C. § 103(a) based on the combination of Crocker et al., Nale, and Reddy should be reversed because the Examiner has failed to establish a prima facie case of obviousness with regard to claims 1-13 and 15-30. More specifically, for at least the reasons stated below, no proper combination of Crocker et al., Nale, and Reddy teaches or suggests the subject matter of claims 1-13 and 15-30.

A. The Examiner's Rejection of Claims 1-13 and 15-30 Should Be Reversed Because the Combination of Crocker et al., Nale, and Reddy Does Not Teach or Suggest At Least One Element of Each of Claims 1-13 and 15-30.

A prima facie case of obviousness requires that the prior art reference or references teaches or suggests all of the claimed limitations. In re Royka, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974). The combination of Crocker et al., Nale, and Reddy does not teach or suggest at

least one element of each of claims 1-13 and 15-30. Accordingly, the Examiner has failed to establish a prima facie case of obviousness, and the rejection of claims 1-13 and 15-30 should be reversed.

Independent claims 1, 15, and 22 each recite in combination with other limitations "dedicated internal display random access memory ..., a dedicated external display random access memory ..., the display logic being configured to manage the internal and external display random access memory and allocate the internal and external display random access memory across the internal and external display random access memory according to the display mode ... the display modes including at least one of resolution modes and color modes." The cited combination of Crocker et al., Nale, and Reddy does not teach or suggest "dedicated internal display random access memory ..., a dedicated external display random access memory ..., the display logic being configured to manage the internal and external display random access memory and allocate the internal and external display random access memory across the internal and external display random access memory according to the display mode ... the display modes including at least one of resolution modes and color modes" as included in the respective combinations of elements of claim 1, claim 15, or claim 22.

In the final Office Action dated July 1, 2005, the Examiner acknowledged that "the combined system [of Crocker et al. and Nale] fails to explicitly teach or suggest the memory includes an internal RAM and an external RAM for allocating between the two." However, the Examiner further stated that "Reddy teaches an integrated graphics display memory element including both a graphics accelerator (110) and an on chip frame buffer (112) and an off chip frame buffer (114). The graphics accelerator distributes and/or controls both the internal and external RAMs." Thus, as admitted by the Examiner, neither Crocker et al. nor Nale disclose an internal random access memory and an external random access memory, much less an internal random access memory and an external random access memory configured in accordance with the subject matter of claims 1, 15, or 22. The Examiner relies on Reddy to disclose or suggest an internal random access memory and an external random access memory.

Reddy, however, discloses only that an on-chip DRAM portion 112 and an off-chip DRAM portion 114 may be utilized to store a faster moving image portion onto the on-chip DRAM portion 112 while storing a slower moving image portion onto the on-chip DRAM portion 112, to accommodate different CRT sizes (See Reddy, col. 3, lines 22-50), to separately manage even and odd lines or subsections of a CRT display (See Reddy, col. 4, lines 56-67), or to store and repair faulty frame buffer bits (See Reddy, col. 5, lines 1-23). These uses of an off-chip DRAM portion 114 taught by Reddy are not a teaching of managing or allocating internal and external random access memory configurations according to color or resolution display modes. Thus, the cited combination of Crocker et al., Nale, and Reddy does not teach or suggest "dedicated internal display random access memory ..., a dedicated external display random access memory ..., the display logic being configured to manage the internal and external display random access memory and allocate the internal and external display random access memory across the internal and external display random access memory according to the display mode ... the display modes including at least one of resolution modes and color modes" as included in the respective combinations of elements of claim 1, claim 15, or claim 22. Therefore, it is respectfully submitted that the Examiner has failed to establish a prima facie case of obviousness because the combination of Crocker et al., Nale, and Reddy does not teach or suggest at least one element of each of claims 1, 15, and 22, and that and the rejection of claims 1, 15, and 22 should be reversed.

Claims 2-13 depend from independent claim 1, claims 16-21 depend from independent claim 15, and claims 23-30 depend from claim 22 and are therefore patentable for at least the same reasons as discussed above. See 35 U.S.C. § 112 ¶ 4.

B. The Examiner's Rejection of Claims 1-13 and 15-30 Should Be Reversed Because There Is No Suggestion to Combine the Teachings of Crocker et al., Nale, and Reddy

To establish a prima facie case of obviousness based on a combination of prior art references under 35 U.S.C. § 103(a), the Examiner must first show that there is a suggestion or motivation to combine the teachings of these references. To satisfy this burden, the Examiner

must show some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references. In re Fritch, 972 F.2d 1260 (Fed. Cir. 1992). When the motivation to combine the teachings of the references is not immediately apparent, it is the duty of the Examiner to explain why the combination of the teachings is proper. Ex parte Skinner, 2 U.S.P.Q.2d 1788 (Bd. Pat. App. & Inter. 1986). In this case, the Examiner has not shown – and indeed, cannot show, that there would have been any motivation or suggestion to combine the teachings of Crocker et al., Nale, and Reddy.

In the final Office Action dated July 1, 2005, the Examiner acknowledged that "the combined system [of Crocker et al. and Nale] fails to explicitly teach or suggest the memory includes an internal RAM and an external RAM for allocating between the two." However, the Examiner further stated that "Reddy teaches an integrated graphics display memory element including both a graphics accelerator (110) and an on chip frame buffer (112) and an off chip frame buffer (114). The graphics accelerator distributes and/or controls both the internal and external RAMs." The Examiner concluded that:

> It would have been obvious to one of ordinary skill in the art at the time the present invention was made to combine the teachings of internal and external RAMs into the combined system of Crocker and Nale in order to increase the performance of the graphics display system because display data retrieval from on-chip frame buffer is much faster from external frame buffer and also reduce on-chip power dissipation that is especially critical in hand held portable, possibly wireless, products where battery life is a primary essential operational issue; and thus achieving system performance. The integrated solution also allows the display memory sign to be expanded by adding external memory so that large displays can be accommodated on an as needed basis as taught by Reddy (col. 2, lines 30-41 and col. 4, lines 1-20). Therefore, at least claims 1-4 and 15-30 would have been obvious.

While Reddy discloses that "display data retrieval from the on-chip frame buffer is much faster from an external frame buffer" (see Reddy, col. 2, lines 31-33), mentions reducing or

increasing power dissipation based on refresh frequency (see Reddy, col. 3, line 57 – col. 4, line 20), and discloses that the "integrated solution also allows the display memory size to be expanded by adding external memory so that large displays can be accommodated on an as needed basis" (see Reddy, col. 2, lines 35-38), it is unclear how the Examiner's statement provides a motivation to combine the teachings of Reddy with those of Crocker et al. Rather, the Examiner's statement merely suggests that advantages described in Reddy may also be obtained if Crocker et al. and Nale are somehow modified to include components of Reddy (e.g., the on-chip DRAM portion 112 and off-chip DRAM portion 114). However, the Examiner has not provided any indication (nor do Crocker et al., Nale, or Reddy teach or suggest) how the teachings of Crocker et al. and Nale would have to be modified to include the teachings of Reddy to achieve such advantages, or how the on-chip DRAM portion 112 and off-chip DRAM portion 114 would work with any system taught by Crocker et al. or Nale. Further, there is no teaching or suggestion in Crocker et al., Nale, or Reddy that their teachings are compatible with each other.

As such, the Examiner's statements regarding the motivation to combine Crocker et al., Nale, and Reddy do not evince the "thorough and searching inquiry" required by the U.S. Court of Appeals for the Federal Circuit. See McGinley v. Franklin Sports, Inc., 262 F.3d 1339, 60 U.S.P.Q.2d 1001 (Fed. Cir. 2001). Instead of properly describing a motivation to combine the teachings of Crocker et al., Nale, and Reddy, the Examiner has engaged in hindsight reasoning to combine such teachings. Here, the Examiner has used Appellants' patent application as a road map to make such a combination. The hindsight reconstruction engaged in by the Examiner is improper where there is no showing that it is based on knowledge that was within the level of ordinary skill in the art at the time the claimed invention was made and includes knowledge gleaned only from Appellants' disclosure. See M.P.E.P § 2145, Section X, Subsection A.

In fact, Crocker et al. teaches away from the teachings of Reddy. It is improper to combine references where the references teach away from their combination. See In re Grasselli, 713 F.2d 731, 743, 218 U.S.P.Q. 769, 779 (Fed. Cir. 1983). Crocker et al., when viewed as a

whole, teaches only a shared memory buffer architecture in which a single physical memory is shared between dedicated memory allocated for use by one or more devices (e.g., graphics controller 5) and system memory available to the operating system. See Crocker et al., col. 3, lines 41-47. Crocker et al., when viewed as a whole, also teaches providing "graphical support on the motherboard without requiring the expense of a corresponding add-in dedicated memory." See Crocker et al., col. 2, lines 50-52. In contrast, Reddy teaches the use of two memory devices dedicated for use as frame buffers – an on-chip DRAM frame buffer 112 and off-chip DRAM frame buffer 114. See Reddy, col. 3, lines 13-18. Thus, the teachings of Crocker et al. regarding use of a single shared memory device to avoid the additional cost of additional dedicated memory devices teach away from combination with Reddy's use of an on-chip DRAM frame buffer 112 and off-chip DRAM frame buffer 114, and such combination of the teachings of Crocker et al. with those of Reddy is therefore improper.

Crocker et al. also teaches away from the subject matter of claims 1, 15, and 22. When a reference teaches away from the claimed invention, that teaching is strong evidence of non-obviousness. See U.S. v. Adams, 383 U.S. 39, 148 U.S.P.Q. 79 (1966); In re Royka, 490 F. 2d 981, 180 U.S.P.Q. 580 (CCPA 1974). In contrast with the teachings of Crocker et al., claims 1, 15, and 22 each recite a "dedicated internal display random access memory" and "a dedicated external display random access memory." The teachings of Crocker et al. regarding use of a single shared memory device to avoid the additional cost of additional dedicated memory devices teach away from the use of a "dedicated internal display random access memory" and "a dedicated external display random access memory" as recited in claims 1, 15, and 22, and as such, the teachings of Reddy provide strong evidence of non-obviousness.

The proposed combination of the teachings of Reddy with those of Crocker et al. would also change the principle of operation of Crocker et al. If the proposed combination of the references would change the principle of operation of the reference being modified, the teachings of the references are not sufficient to render the claims prima facie obvious. See In re Ratti, 270 F.2d 810, 123 U.S.P.Q. 349 (C.C.P.A. 1959). The device of Crocker et al. uses a single shared

memory device to provide a both a frame buffer and system memory available to the operating system while avoiding the added cost of additional dedicated memory devices. To modify the device of Crocker et al. to include the on-chip DRAM frame buffer 112 and off-chip DRAM frame buffer 114 would require a substantial and unnecessary redesign of the device of Crocker et al. and would change the principle of operation under which the architecture of Crocker et al. was designed to operate (i.e., a single shared memory device to provide a both a frame buffer and system memory available to the operating system). Thus, the combined teachings of Crocker et al. and Reddy are not sufficient to render the subject matter of claims 1, 15, and 22 prima facie obvious.

Furthermore, Appellants note that the Examiner's purported motivations for combining the teachings of Reddy with those of Crocker et al. and Nale (i.e., speed and power savings) would not motivate one of ordinary skill in the art to use an off-chip/on-chip structure such as the on-chip DRAM portion 112 and off-chip DRAM portion 114 taught in Reddy. Rather, one of ordinary skill in the art would be motivated one to simply use an entirely on-chip structure to obtain speed and power savings.

Therefore, it is respectfully submitted that the Examiner has failed to establish a prima facie case of obviousness because there is no suggestion or motivation to combine the teachings of Crocker et al., Nale, and Reddy, and that and the rejection of claims 1, 15, and 22 should be reversed.

Claims 2-13 depend from independent claim 1, claims 16-21 depend from independent claim 15, and claims 23-30 depend from claim 22 and are therefore patentable for at least the same reasons as discussed above. See 35 U.S.C. § 112 ¶ 4.

8. CONCLUSION

In view of the foregoing, Appellants submit that claims 1-13 and 15-30 are not properly rejected under 35 U.S.C. § 103(a) as being unpatentable over Crocker et al., Nale, and Reddy and

are therefore patentable. Accordingly, Appellants respectfully request that the Board reverse all claim rejections and indicate that a notice of allowance respecting all pending claims should be issued.

Respectfully submitted,

Date 12/5/2005 By Chad E. Bement

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CLAIMS APPENDIX

1. A computing device, comprising:

a communications bus;

a display configured to display in more than one display mode and coupled to the communications bus;

a processor, coupled to the display and to the communications bus; and

a display controller coupled to the communications bus and having dedicated internal display random access memory, the internal display random access memory being used for storing display information, the internal display random access memory configured to receive and provide access to display information to be communicated to the display, the internal display random access memory being controlled by display logic; and

a dedicated external display random access memory coupled to the display controller, the display logic being configured to manage the internal and external display random access memory and allocate the internal and external display random access memory across the internal and external display random access memory according to the display mode and the display logic is configured to change the display mode during operation of an application running on the computing device according to changing graphical needs of the application, the display modes including at least one of resolution modes and color modes.

2. The computing device of claim 1, wherein the display mode is initiated dependent upon the application running on the processor.

3. The computing device of claim 1, wherein the display mode is dependent upon the available memory.

4. The computing device of claim 1, wherein the display mode is dependent upon the available memory bandwidth.

5. The computing device of claim 1, wherein the more than one display mode includes a high resolution display mode.

6. The computing device of claim 1, wherein the more than one display mode includes a low resolution display mode.

7. The computing device of claim 1, wherein the more than one display mode includes a 18 bit color display mode.

8. The computing device of claim 1, wherein the more than one display mode includes a 24 bit color display mode.

9. The computing device of claim 1, wherein the more than one display mode includes an 8 bit display mode.

10. The computing device of claim 1, wherein the more than one display mode includes a display mode having up to 25,600 pixels.

11. The computing device of claim 1, wherein the more than one display mode includes a display mode having up to 102,400 pixels.

12. The computing device of claim 1, wherein the more than one display mode includes a text display mode.

13. The computing device of claim 1, wherein the more than one display mode includes a monochrome display mode.

15. A personal digital assistant, comprising:

a communication bus;

a display configured to display in more than one display mode and coupled to the communications bus;

a processor, coupled to the display and to the communications bus; and

a display controller coupled to the communications bus and having dedicated internal display random access memory, the internal display random access memory being used for storing display information, the internal display random access memory configured to receive and provide access to display information to be communicated to the display, the internal display random access memory being controlled by display logic; and

a dedicated external display random access memory coupled to the display controller, the display logic being configured to manage the internal and external display random access memory and allocate the internal and external display random access memory across the internal and external display random access memory according to the display mode and the display logic is configured to change the display mode during operation of an application running on the computing device according to changing graphical needs of the application, the display modes including at least one of resolution modes and color modes.

16. The personal digital assistant of claim 15, wherein the display mode is initiated dependent upon the application running on the processor.

17. The personal digital assistant of claim 15, wherein the display mode is dependent upon a mode signal from the operating system.

18. The personal digital assistant of claim 15, wherein the display mode is dependent upon the display requirements of an application running on the processor.

19. The personal digital assistant of claim 15, wherein the display includes a touch screen.

20. The personal digital assistant of claim 15, wherein the unified memory includes random access memory (RAM).

21. The personal digital assistant of claim 15, wherein further comprising:

a display controller, wherein the display controller is configured to perform the display logic.

22. A computing device, comprising:

a communications bus;

a display configured to display in more than one display mode and coupled to the communications bus;

a processor, coupled to the display and to the communications bus;

a display controller coupled to the communications bus and having dedicated internal display random access memory, the internal display random access memory being used for storing display information, the internal display random access memory configured to receive and provide access to display information to be communicated to the display, the internal display random access memory being controlled by display logic; and

a dedicated external display random access memory coupled to the display controller, the display logic being configured to manage the internal and external display random access memory and allocate the internal and external display random access memory across the internal and external display random access memory according to the display mode and the display logic is configured to change the display mode during operation of an application running on the computing device according to changing graphical needs of the application, the display modes including at least one of resolution modes and color modes.

23. The computing device of claim 22, wherein the display mode is initiated dependent upon the application running on the processor.

24. The computing device of claim 22, wherein the display mode is dependent upon a mode signal from the operating system.

25. The computing device of claim 22, wherein the display mode is dependent upon the display requirements of an application running on the processor.

26. The computing device of claim 22, wherein the display includes a touch screen.

27. The computing device of claim 22, wherein the unified memory includes random access memory (RAM).

28. The computing device of claim 22, wherein the computing device is included in a personal digital assistant.

29. The computing device of claim 22, wherein the computing device is included in a cellular phone.

30. The computing device of claim 22, wherein the computing device is included in a handheld device.

EVIDENCE APPENDIX

None

RELATED PROCEEDINGS APPENDIX

None